

Amendment and Response

Applicant: Jonghee Han et al.

Serial No.: 10/674,177

Filed: September 29, 2003

Docket No.: 2003P52606US/I436.103.101

Title: RANDOM ACCESS MEMORY WITH POST-AMBLE DATA STROBE SIGNAL NOISE REJECTION

IN THE CLAIMS

Please cancel claims 2, 3, 9-22, 26, and 31.

Please add claims 32-34.

Please amend claims 1, 23, and 27 as follows:

1. (Currently Amended) A random access memory, comprising:
a first circuit configured to receive a strobe signal and provide pulses in response to transitions in the strobe signal; and
a second circuit configured to receive the strobe signal to latch data into the second circuit in response to the strobe signal, and to receive the pulses to re-latch~~latch~~ the latched data into the second circuit after the transitions in the strobe signal,
wherein the first circuit comprises:
an enable circuit configured to provide an enable signal; and
a buffer circuit configured to receive the strobe signal and the enable signal
and provide the pulses in response to the enable signal and the strobe signal,
wherein the enable circuit is configured to receive the pulses from the buffer
circuit and stop providing the enable signal to the buffer circuit in response to
receiving the pulses.
- 2-3. (Cancelled)
4. (Original) The random access memory of claim 1, wherein the first circuit provides one of the pulses during each cycle of the strobe signal and each cycle of a clock signal.
5. (Original) The random access memory of claim 1, wherein the second circuit comprises:
a first latch configured to latch first data at first transitions in the strobe signal; and
second latches configured to latch the latched first data from the first latch and second data at second transitions in the strobe signal.

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6. (Original) The random access memory of claim 5, wherein the second circuit comprises:

third latches configured to latch in the latched first and second data from the second latches with the pulses after the second transitions.

7. (Original) The random access memory of claim 1, wherein the memory comprises a double data rate-I synchronous dynamic random access memory.

8. (Original) The random access memory of claim 1, wherein the memory comprises a double data rate-II synchronous dynamic random access memory.

9-22. (Cancelled)

23. (Currently Amended) A random access memory, comprising:

means for generating a pulse after a transition in a data strobe signal;

means for latching data using the data strobe signal; and

means for latching the latched data using the pulse,

wherein the means for latching the latched data comprises a third latch stage configured to receive the pulse and latch the latched data into the third latch stage.

24. (Original) The random access memory of claim 23, wherein the means for generating a pulse comprises a means for generating the pulse after a falling edge of the data strobe signal and before a rising edge of the data strobe signal.

25. (Original) The random access memory of claim 23, wherein the means for latching data comprises:

means for latching data at a rising edge of the data strobe signal;

means for latching data at a falling edge of the data strobe signal; and

means for latching latched data with the data strobe signal.

26. (Cancelled)

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27. (Currently Amended) A method for rejecting post-amble noise on a data strobe signal in a random access memory, comprising:

generating a pulse before the data strobe signal floats; and

latching data into a latch stage with the pulse to preserve the data,

wherein generating the pulse comprises:

receiving a signal at an enable circuit;

generating an enable signal from a transition on the received signal;

receiving the enable signal and the data strobe signal at a buffer circuit;

generating a start of the pulse based on the received enable signal and the received data strobe signal; and

receiving the start of the pulse at the enable circuit.

28. (Original) The method of claim 27, wherein generating the pulse comprises generating the pulse during each cycle of the data strobe signal and each cycle of a clock signal.

29. (Original) The method of claim 27, wherein generating the pulse comprises generating the pulse after a falling edge of the data strobe signal.

30. (Original) The method of claim 27, wherein generating the pulse comprises:
generating an enable signal; and
generating a start of the pulse based on the enable signal and the data strobe signal.

31. (Cancelled)

32. (New) A random access memory, comprising:
a first circuit configured to receive a strobe signal and provide pulses in response to transitions in the strobe signal; and
a second circuit configured to receive the strobe signal to latch data into the second circuit in response to the strobe signal, and to receive the pulses to re-latch the latched data into the second circuit after the transitions in the strobe signal,

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wherein the second circuit comprises:

a first latch configured to latch first data at first transitions in the strobe signal;
second latches configured to latch the latched first data from the first latch and
second data at second transitions in the strobe signal; and
third latches configured to latch in the latched first and second data from the
second latches with the pulses after the second transitions.

33. (New) A random access memory, comprising:

a first circuit configured to receive a strobe signal and a clock signal and to provide
pulses in response to transitions in the strobe signal, wherein the first circuit is configured
such that only one pulse is provided in response to a transition in the strobe signal after each
edge of a predetermined type of the clock signal; and

a second circuit configured to receive the strobe signal to latch data into the second
circuit in response to the strobe signal, and to receive the pulses to re-latch the latched data
into the second circuit after the transitions in the strobe signal.

34. (New) A method for rejecting post-amble noise on a data strobe signal in a random
access memory, comprising:

receiving the strobe signal and a clock signal;
generating pulses in response to transitions in the strobe signal such that only one
pulse is provided in response to a transition in the strobe signal after each edge of a
predetermined type of the clock signal;

receiving the strobe signal to latch data into a second circuit; and
receiving the pulses to re-latch the latched data into the second circuit after the
transitions in the strobe signal.